[**Input Unit and Memory Address Register (MAR):**](https://www.youtube.com/watch?v=DHD99TvLEVA&list=PLk4sSigu0N0W4v755N_O6Jk1WWrfWIGgm&index=2)

A computer diagram of a computer

Description automatically generated with medium confidence

A diagram of a computer

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The Memory Address Register (MAR) is a register designed to store the memory address that the CPU needs to access in order to read or write data from the computer's memory. Essentially, it holds the address of the specific memory location currently in use by the CPU.

When the CPU requires data retrieval from or data storage into a particular memory location, it loads the relevant memory address into the MAR. This address then serves as the means to identify and access the appropriate memory location for data transfer.

Normally, the MAR is preloaded with the memory address before the actual memory access operation occurs. It plays a crucial role in the SAP-1 computer's fetch-decode-execute cycle, where the CPU retrieves both instructions and data from memory.

Within the SAP-1 architecture, the MAR is an 8-bit register, meaning it can store an 8-bit binary value that represents a memory address. This capability enables the SAP-1 to access a maximum of 256 memory locations, as 2^8 equals 256.